Abstracts

Design of Clock Recovery MMIC Using Large-Signal Computer-Aided Analysis

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Next generation of Gb/s local area distribution networks employed as optical interconnects are designed using OEIC technology for low power consumption, high reliability, and low cost. A hybrid optoelectronic integrated circuit (OEIC) integrated with MMIC circuits is described in this paper as a first step toward full monolithic integration. Si MMIC foundry services from Bipolarics was selected to design an optical receiver with an injection locked phase lock loop (ILPLL) clock recovery circuit at 1.25 Gb/s. The simulation has indicated that the input noise equivalent voltage density of the receiver is lower than 0.6 nV/radic Hz for frequency up to 1 GHz. The simulated minimum received optical power to extract the clock signal is -30 dBm. The output clock signal of this clock recovery circuit is about 400 mV/sub p-p. Simulated power consumption is 630 mW for the optical receiver and the ILPLL clock recovery circuit.

❑ Return to main document.